Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently amended) A non-volatile semiconductor memory device comprising:

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

and wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data.

2. (Currently amended) The non-volatile semiconductor memory device according to claim 1, wherein

each of said sense amplifier circuits further comprises:

~~a first latch circuit for holding a read data of said first memory cell;~~

~~a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data;~~

a first sense node connected to a bit line of said memory cell array via a clamping transistor used for clamping and amplifying bit line potential;

a second sense node to which said first and second latch circuits are commonly connected through the respective transfer gates; and

first and second data transfer circuits disposed in parallel between said first and second sense nodes, said first and second data transfer circuits being switched in response to said reference data held in said second latch circuit to selectively transfer one of cell data of said first memory cell under first and second read conditions to said first latch circuit.

3. (Original) The non-volatile semiconductor memory device according to claim 2, wherein

said first and second read conditions are determined by changing a read voltage applied to said first memory cell.

4. (Original) The non-volatile semiconductor memory device according to claim 2, wherein

said first and second read conditions are determined as corresponding to differences of bit line discharge times determined due to said first memory cell.

5. (Original) The non-volatile semiconductor memory device according to claim 2, wherein

said first data transfer circuit comprises first and second transistors serially disposed between said first and second sense nodes, said first transistor being gate-controlled by a first data node of said second latch circuit, said second transistor being driven by a first sense-use control signal to turn on, and wherein

said second data transfer circuit comprises third and fourth transistors serially disposed between said first and second sense nodes, said third transistor being gate-controlled by a second data node of said second latch circuit, said fourth transistor being driven by a second sense-use control signal to turn on, said second sense-use control signal being generated at a timing different from that of said first sense-use control signal.

6. (Original) The non-volatile semiconductor memory device according to claim 2, wherein

each said sense amplifier circuit further comprises:

a first precharge transistor connected to said first sense node for precharging a selected bit line of said memory cell array; and

a second precharge transistor connected to said second sense node for precharging said second sense node.

7. (Original) The non-volatile semiconductor memory device according to claim 1, wherein

said memory cell array comprises a plurality of NAND cell units arranged therein, each NAND cell unit having a serial circuit of a plurality of memory cells, a first select gate transistor disposed between one end of said serial circuit and a bit line, and a second select gate transistor disposed between the other end of said serial circuit and a common source line, each said memory cell having a floating gate and a control gate stacked thereabove.

8. (Original) The non-volatile semiconductor memory device according to claim 7, wherein

the control gates of said memory cells in each said NAND cell unit are connected to different word lines, respectively, and wherein

the gates of said first and second select gate transistors in each said NAND cell unit are connected to select gate lines, respectively.

9. (Currently amended) The non-volatile semiconductor memory device according to claim 8, wherein

a plurality of memory cells arranged along a word line and connected to different bit lines, respectively, constitute a page which serves as a unit for parallel data read and parallel ~~dada~~ data write, and wherein

said plurality of sense amplifier circuits constitute a page buffer for sensing data of one page.

10. (Currently amended) A memory system comprising:

a non-volatile semiconductor memory device ~~defined in claim 1~~;

a cache memory for temporarily storing data input to and output from said non-volatile semiconductor memory device; and

a controller for controlling ~~dada~~ data transfer between said cache memory and said non-volatile semiconductor memory device in such a manner that a data rewrite operation of said non-volatile semiconductor memory device is performed for a rewrite region directed from external in order from the uppermost address of said rewrite region,

wherein said nonvolatile memory device comprises:

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

and wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data.

11. (Original) The memory system according to claim 10, wherein

said non-volatile semiconductor memory device comprises a plurality of cell blocks each serving as a unit for a data erase in a lump, and wherein

said cache memory has a data storing area with a capacity larger than that of each said cell block, and wherein

said controller controls to store data, which is to be written into a cell block of said non-volatile semiconductor memory device, in said cache memory, and then transfer the stored data to said non-volatile semiconductor memory device, thereby starting a data write operation.

12. (Currently amended) An electric card equipped with a non-volatile semiconductor memory device, wherein said non-volatile memory device comprises: ~~defined in claim 1~~.

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

and wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data.

13. (Currently amended) An electric card equipped with a memory system ~~defined in claim 11~~ comprising:

a non-volatile semiconductor memory device,

a cache memory for temporarily storing data input to and output from said non-volatile semiconductor memory device; and

a controller for controlling data transfer between said cache memory and said non-volatile semiconductor memory device in such a manner that a data rewrite operation of said non-volatile semiconductor memory device is performed for a rewrite region directed from external in order from the uppermost address of said rewrite region;

wherein said non-volatile semiconductor memory device comprises:

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data,

wherein said non-volatile semiconductor memory device comprises a plurality of cell blocks each serving as a unit for a data erase in a lump, and wherein

said cache memory has a data storing area with a capacity larger than that of each said cell block, and wherein

said controller controls to store data, which is to be written into a cell block of said non-volatile semiconductor memory device, in said cache memory, and then transfer the stored data to said non-volatile semiconductor memory device, thereby starting a data write operation.

14. (Currently amended) An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card ~~defined in claim 12 and~~ electrically connectable to said card slot, wherein said electric card is equipped with a non-volatile semiconductor memory device, wherein said non-volatile memory device comprises:

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

and wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data.

15. (Currently amended) An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card ~~defined in claim 13 and~~ electrically connectable to said card slot, wherein said electric card is equipped with a memory system comprising:

a non-volatile semiconductor memory device,

a cache memory for temporarily storing data input to and output from said non-volatile semiconductor memory device; and

a controller for controlling data transfer between said cache memory and said non-volatile semiconductor memory device in such a manner that a data rewrite operation of said non-volatile semiconductor memory device is performed for a rewrite region directed from external in order from the uppermost address of said rewrite region;

wherein said non-volatile semiconductor memory device comprises:

a memory cell array in which electrically rewritable floating gate type memory cells are arranged; and

a plurality of sense amplifier circuits configured to read data from said memory cell array, wherein

each of said sense amplifier circuits is configured to sense cell data of a first memory cell selected from said memory cell array under a read condition

determined in correspondence with cell data of a second memory cell adjacent to said first memory cell and written after said first memory cell,

and wherein each said sense amplifier circuit comprises a first latch circuit for holding a read data of said first memory cell and a second latch circuit for holding a data read out from said second memory cell prior to data read of said first memory cell as a reference data.

16. (Original) The electric device according to claim 14, wherein said electric device is a digital still camera.

17. (Original) The electric device according to claim 15, wherein said electric device is a digital still camera.